Docket No.: P2002,0892

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

By: _____ Date: May 6, 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applic. No.	:	10/689,419	Confirmation No: 2800
Applicant	:	Martin Perner	
Filed	:	October 20, 2003	
Title	:	Semiconductor Module and Methods for Functionally Testing and Configuring a Semiconductor	
Art Unit	:	2812	
Examiner	:	to be assigned	
Docket No.	:	P2002,0892	
Customer No.	:	24131	

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner for Patents

S i r :

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

Dae-Young Jung et al. :Reusable Embedded Debugger for 32bit RISC Processor Using the JTAG Boundary Scan Architecture", Proceedings of the 2002 IEEE Asia Pacific Conference on ASIC, 2002, pp. 209-212;

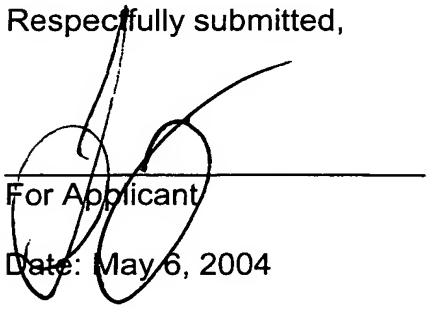
E. de la Torre et al.: "Non-intrusive debugging using the JTAG interface of FPGA-based prototypes", Proceedings of the 2002 IEEE International Symposium on Industrial Electronics, 2002, pp. 666-671;

German Examination Report dated March 23, 2004.

In accordance with 37 C.F.R. 1.97(e) the undersigned herewith states that each item of information contained in the information disclosure statement was first cited in a

communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement.

Respectfully submitted,



Gregory L. Mayback
Reg. No. 40,719

For Applicant

Date: May 6, 2004

Lerner And Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

/bmb

FORM PTO-1449 (SUBSTITUTE)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE
STATEMENT BY APPLICANT
(37 CFR 1.98(b))

Attorney Docket No.:	Applic. No.
P2002,0892	10/689,419

Applicant: Martin Perner

Filing Date	Group Art Unit
October 20, 2003	2812

U.S. PATENT DOCUMENTS

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A						
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J							
	K							
	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	O	Dae-Young Jung et al. :Reusable Embedded Debugger for 32bit RISC Processor Using the JTAG Boundary Scan Architecture", Proceedings of the 2002 IEEE Asia Pacific Conference on ASIC, 2002, pp. 209-212
	P	E. de la Torre et al.: "Non-intrusive debugging using the JTAG interface of FPGA-based prototypes", Proceedings of the 2002 IEEE International Symposium on Industrial Electronics, 2002, pp. 666-671

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.